

电子 Technology

RISC-V 2025 中国峰会关键议题解读（1）：从嵌入式走向高性能计算，自主架构的战略跃升之路

Key Topics from the 2025 RISC-V China Summit (1): From Embedded Systems to High-Performance Computing—The Strategic Leap of an Independent Architecture

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Flash Analysis

(Please see APPENDIX 1 for English summary)

事件：

2025 年 RISC-V 中国峰会显示，RISC-V 指令集架构向高性能计算（HPC）领域的演进，正成为半导体产业发展的重要转折点。这标志着 RISC-V 从嵌入式和端侧应用逐渐转变为高性能、通用算力领域的战略级技术路线，重新定义了芯片产业自主可控和开放创新的格局。

点评：

RISC-V 架构正在推动芯片生态从嵌入式领域走向高性能计算领域的战略跃升。从传统“嵌入式应用为主”的架构，逐渐演变为具备规模化商用潜力的高性能通用计算平台。这意味着 RISC-V 不再仅仅适用于边缘设备、传感器等简单应用场景，而是逐步具备了支撑数据中心、AI 计算、汽车电子等核心领域的实力。芯来科技创始人胡振波在峰会上指出：“RISC-V 在 AI 计算、汽车电子、高性能通用处理三大领域都即将实现关键突破，产业生态正在逐步成熟。”

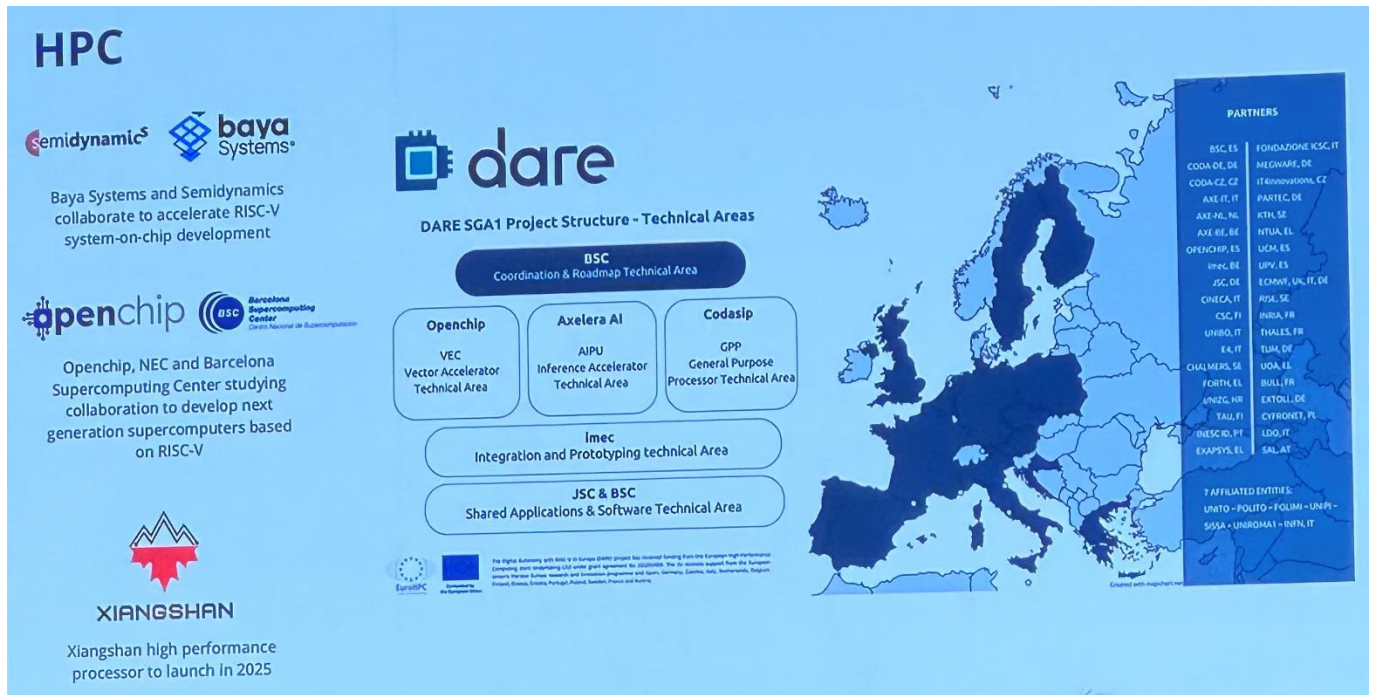
RISC-V 生态正逐步构建起以多核异构计算为特征的新计算范式。不同于传统处理器依靠单一架构提供所有计算能力，RISC-V 生态鼓励厂商基于开放架构自行定制，以形成“通用算力核+专用加速核”的多核异构架构。例如，英伟达在峰会上介绍了将 CUDA 工具链移植至 RISC-V 的计划，其 NVLink Fusion 技术通过 RISC-V CPU 与 GPU、网络芯片的异构融合，实现数据中心级应用的高效能扩展。RISC-V 领域的领先芯片企业 Tenstorrent 推出了 Blackhole AI 芯片，该芯片采用由 16 个高性能 RISC-V 大核和 752 个 RISC-V 小核组成的计算矩阵架构。其中，16 个大核负责通用计算任务，752 个 Baby RISC-V 内核则用于专门加速计算。据官方介绍，这款新品的计算性能可达 745 TOPS，在整体 AI 处理能力和扩展性方面甚至超过了英伟达的 A100 芯片。

RISC-V 架构的核心竞争力将逐步从“开放性”转变为“高效能执行力”。过去几年，产业界强调 RISC-V 架构的开源特性、可扩展性与定制化优势，而此次峰会的共识则是，未来决定 RISC-V 成败的关键在于其能否在高性能、复杂任务场景持续稳定运行。算能科技推出的高性能 RISC-V 处理器 SG2042 与 SG2044，正是通过将异构计算单元整合到芯片内部，实现片内的高效协同，以确保 RISC-V 芯片在实际应用中具备真正的性能竞争力。

我们认为，RISC-V 架构迈向高性能计算领域的战略转型，将成为未来芯片产业自主创新的重要突破口。从嵌入式应用到数据中心级别算力核心，从专用控制场景到通用任务处理能力的跃升，RISC-V 正在深刻改变芯片产业竞争格局。未来的竞争将逐渐从“谁的架构开放性更高”，转向“谁能真正落地通用高性能应用并建立完整生态闭环”。长远来看，RISC-V 有望成为媲美 ARM 和 x86 的下一代主流架构平台，一旦高性能计算领域的生态建设完成，将迅速推动产业转型，催生一批新的半导体企业和生态合作伙伴。

风险提示：1) AI 需求不及预期；2) 地缘政治环境干扰供应链；3) AI 数据中心建造放缓

Fig.1 RISC-V 高性能计算生态合作与项目布局概览



Source: RISC-V 2025, HTI

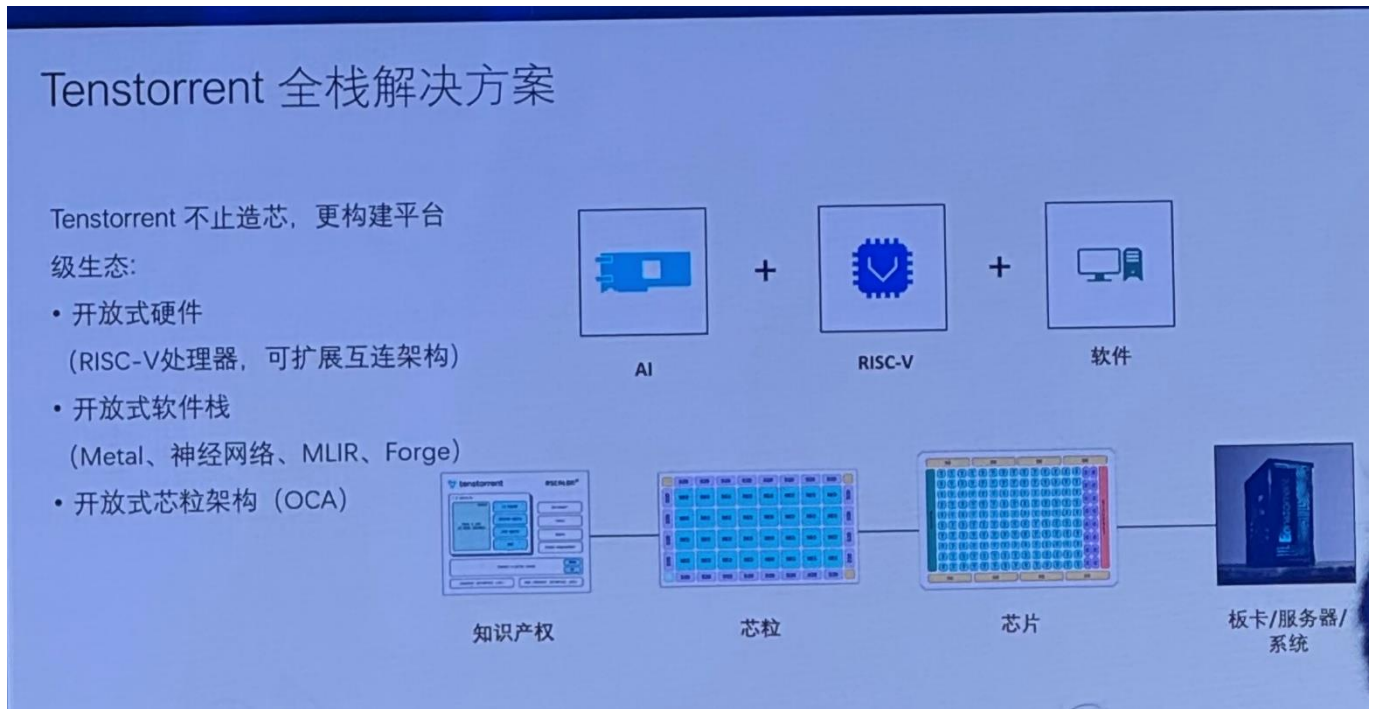
Fig.2 RISC-V Linux 生态加速

Linux Support for RISC-V is accelerating fast!

- Official RISC-V Yocto Images
- Full positive test coverage will be required before release
- Long Term Support (LTS) releases for 4 years
- Support for all RISC-V profiles
- RISC-V representative on Governing Board
- Developer preview of Red Hat Enterprise Linux (RHEL) 10 for RISC-V
- Running on the SiFive HiFive Premier P550 platform
- Enables evaluation of RISC-V for AI, infrastructure, enterprise, edge and embedded workloads
- Available for download now!
- DC-ROMA RISC-V Laptop II - world's first RISC-V laptop pre-installed and powered by Ubuntu
- Canonical has brought Ubuntu to multiple RISC-V development boards
- Rivos and Canonical partnered to deliver scalable RISC-V solutions in Data Centers and enable an enterprise-grade Ubuntu experience across Rivos platforms

Source: RISC-V 2025, HTI

Fig.3 Tensorrent 全栈开放生态: RISC-V 芯粒架构与 AI 软硬件协同平台



Source: Tensorrent, RISC-V 2025, HTI

English Summary:

Event:

At the 2025 RISC-V China Summit, the transition of the RISC-V instruction set architecture toward High-Performance Computing (HPC) emerged as a pivotal development for the semiconductor industry. This shift marks RISC-V's evolution from embedded and edge-oriented applications towards a strategic pathway in high-performance, general-purpose computing, redefining the landscape of autonomous, controllable, and open innovation in the chip industry.

Comments:

The RISC-V architecture is driving a strategic leap within the semiconductor ecosystem from embedded systems to high-performance computing domains. Initially centered around embedded applications, RISC-V is now maturing into a scalable general-purpose computing platform capable of supporting data centers, artificial intelligence computing, automotive electronics, and other core applications. Zhenbo Hu, founder of Nuclei System Technology, highlighted at the summit: "RISC-V is poised for key breakthroughs across AI computing, automotive electronics, and high-performance general-purpose processing, as the ecosystem matures."

RISC-V is progressively fostering a new computational paradigm characterized by heterogeneous multi-core architectures. Unlike traditional processors relying on a single architecture for all computational tasks, the RISC-V ecosystem encourages vendors to customize solutions based on open standards, thus creating multi-core heterogeneous architectures featuring general-purpose computing cores coupled with specialized accelerator cores. For instance, NVIDIA showcased its plan to port the CUDA toolchain to the RISC-V architecture at the summit, leveraging its NVLink Fusion technology to integrate RISC-V CPUs with GPUs and networking chips, enabling efficient scalability for data-center-grade applications. Additionally, Tenstorrent's Blackhole AI chip incorporates a matrix of 16 large cores and 752 smaller cores, establishing an advanced heterogeneous high-performance computing matrix that surpasses the AI performance of NVIDIA's A100, underscoring the strengths of RISC-V in HPC scenarios.

The core competitive advantage of the RISC-V architecture is transitioning from mere "openness" to "efficient execution capability." Over recent years, the industry has emphasized RISC-V's open-source features, extensibility, and customization advantages. However, a key consensus at the summit indicates that future success for RISC-V will hinge on its capacity to perform consistently and stably in high-performance, complex task environments. For example, Semidrive's high-performance RISC-V processors SG2042 and SG2044 integrate heterogeneous computing units within the chip itself, ensuring effective on-chip coordination and thus enhancing practical performance competitiveness.

Nevertheless, the shift of RISC-V from specialized applications to general-purpose computing faces significant challenges, including ecosystem development and performance bottlenecks. YunGang Bao, Chief Scientist at the Beijing Open Source Chip Research Institute, pointed out persistent challenges, such as weak debugging toolchains, slow progress in software mainstreaming, and CPU core performance that lags behind mainstream architectures. Consequently, a systematic approach to ecosystem development and sustained industry resource investment are urgently required to enable the RISC-V architecture's leap from embedded to high-performance computing.

We believe the strategic transformation of the RISC-V architecture towards HPC will represent a crucial breakthrough in autonomous innovation for the future chip industry. Transitioning from embedded applications to data-center-level computing cores, and shifting from specialized control scenarios to general-purpose processing capabilities, RISC-V is reshaping the competitive landscape of the semiconductor industry. Competition will gradually shift from focusing merely on openness towards achieving practical high-performance general-purpose computing and establishing a comprehensive ecosystem. In the long term, RISC-V is likely to emerge as a mainstream architecture comparable to ARM and x86. Once the ecosystem for high-performance computing is fully developed, it will rapidly drive industrial transformation and foster a wave of new semiconductor companies and ecosystem partnerships.

Risk: 1) AI demand falls short of expectations; 2) Geopolitical tensions disrupt supply chains; 3) Slowdown in AI data center construction.

附录 APPENDIX

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